What is claimed is:

1. A method for fabricating a semiconductor device, comprising:
forming a dielectric layer overlaying a semiconductor substrate;
forming an opening in the dielectric layer;
embedding copper or copper alloy into the opening;
forming a silicon layer on the copper or copper alloy by sputtering; and
reacting the silicon layer with the underlying copper or copper alloy to form a copper silicide layer capping the surface of the copper or copper alloy.

2. The method as claimed in claim 1, wherein the dielectric layer comprises a low-k material having k value less than 3.2.

3. The method as claimed in claim 1, wherein the dielectric layer comprises organic low-k material, CVD low-k material, a combination of organic low-k material and CVD low-k material, carbon-containing silicon oxide, nitrogen-containing silicon oxide, FSG, SiC, SiOC or SiOCN.

4. The method as claimed in claim 1, wherein the width of the opening is less than 900Å.

5. The method as claimed in claim 1, wherein the thickness of the embedded copper or copper alloy is less than 4000Å.

6. The method as claimed in claim 1, wherein the silicon layer comprises amorphous silicon.

7. The method as claimed in claim 2, wherein the thickness of the silicon layer is 50 to 500Å.

8. The method as claimed in claim 1, wherein the copper or copper alloy is formed by the steps of:

depositing a copper seed layer in the opening; and

electro-chemical plating or electroless plating the copper or copper alloy on the copper seed layer.

9. The method as claimed in claim 1, wherein the copper or copper alloy is formed by chemical vapor deposition.

10. The method as claimed in claim 1, wherein the copper silicide layer is formed by subjecting the semiconductor substrate to an inert gas-containing ambience at a temperature of about 150 degrees C. to about 450 degrees C.

11. The method as claimed in claim 1, further comprising the steps of:

removing un-reacted portions of the silicon layer; and

forming a diffusion barrier layer overlaying the copper silicide.

12. The method as claimed in claim 11, wherein the diffusion barrier layer comprises silicon-rich oxide, SiN, SiC, SiOC, SiOCN, carbon-containing silicon oxide or nitrogen-containing silicon oxide.

13. The method as claimed in claim 11, further comprising a step of: forming an etch-stop layer overlaying the diffusion barrier layer.

14. The method as claimed in claim 13, wherein the etch-stop layer comprises silicon-rich oxide, SiC, SiOC, SiON, SiOCN, carbon-containing silicon oxide or nitrogen-containing silicon oxide.

15. A method for fabricating a semiconductor device, comprising:
forming a dielectric layer overlaying a semiconductor substrate;
forming an opening in the dielectric layer;
embedding copper or copper alloy into the opening;
forming a silicon layer on the copper or copper alloy by chemical vapor deposition; and
reacting the silicon layer with the underlying copper or copper alloy to form a copper silicide layer capping the surface of the copper or copper alloy.

16. The method as claimed in claim 15, wherein the dielectric layer comprises a low-k material having k value less than 3.2.

17. The method as claimed in claim 15, wherein the dielectric layer comprises an organic low-k material, a CVD low-k material, a combination of organic low-k material and CVD low-k material, carbon-containing silicon oxide, nitrogen-containing silicon oxide, FSG, SiC, SiOC or SiOCN.

18. The method as claimed in claim 15, wherein the width of the opening is less than 900Å.

19. The method as claimed in claim 15, wherein the thickness of the embedded copper or copper alloy is less than 4000Å.

20. The method as claimed in claim 15, wherein the chemical vapor deposition is plasma-enhanced chemical vapor deposition.

21. The method as claimed in claim 15, wherein the silicon layer comprises amorphous silicon.

22. The method as claimed in claim 15, wherein the thickness of the silicon layer is about 50 to 500Å.

23. The method as claimed in claim 15, wherein the copper or copper alloy is formed by the steps of:

depositing a copper seed layer in the opening; and

electro-chemical plating or electroless plating the copper or copper alloy on the copper seed layer.

24. The method as claimed in claim 15, wherein the copper or copper alloy is formed by chemical vapor deposition.

25. The method as claimed in claim 15, wherein the copper silicide layer is formed by subjecting the semiconductor substrate to an inert gas-containing ambience at a temperature of about 150 degrees C. to about 450 degrees C.

26. The method as claimed in claim 15, further comprising the steps of:

removing un-reacted portions of the silicon layer; and

forming a diffusion barrier layer overlaying the copper silicide.

27. The method as claimed in claim 26, wherein the diffusion barrier layer comprises silicon-rich oxide, SiN, SiC, SiOC, SiOCN, carbon-containing silicon oxide, or nitrogen-containing silicon oxide.

28. The method as claimed in claim 26, further comprising a step of: forming an etch-stop layer overlaying the diffusion barrier layer.

29. The method as claimed in claim 28, wherein the etch-stop layer comprises silicon-rich oxide, SiC, SiOC, SiON, SiOCN, carbon-containing silicon oxide or nitrogen-containing silicon oxide.